Basit Malik

basmalik1@gmail.com | 872 803 3772 | LinkedIn | GitHub

Education

University of Illinois at Urbana-Champaign, BS in Computer Engineering — Aug 2025

- **Specialization**: Hardware Systems
- **Coursework:** Computer Organization & Design, Computer Systems Engineering, Digital Systems Lab, Artificial Intelligence, Digital & Analog Signal Processing, Data Structures, Algorithms & Models of Computation

Skills and Technologies

- **Languages:** SystemVerilog, x86, RISC-V, C, C++, C#, Python, JavaScript
- **Tools:** Synopsys VCS & Verdi, FPGA, Quartus, Multisim, Git, Arduino, Linux

Projects

RISC-V Out-of-Order CPU | *SystemVerilog* | *Synopsys VCS & Verdi* | *Waveform Debugging*

- Architected and implemented a Tomasulo-style out-of-order RISC-V CPU supporting RV32I and RV32M
- Pipelined a multi-stage front-end with instruction caching, fetch, decode/rename, and dispatch, enabling register renaming and dynamic stall control
- Integrated reservation station–based scheduling with ROB-controlled in-order retirement across multiple functional units (ALU, MUL, DIV, BR, MEM) to resolve data and structural hazards
- Built constrained-random SystemVerilog testbenches and leveraged waveform tracing using Synopsys VCS and Verdi to validate timing closure and out-of-order execution

Custom Operating System | *C* | *x86* | *QEMU* | *GDB* | *GRUB*

- Engineered a monolithic x86 kernel in C featuring paging-based virtual memory and interrupt-driven I/O
- Programmed Intel 8259 PIC to service hardware interrupts, allowing for keyboard and RTC driver integration
- Routed exceptions and system calls to protect user–kernel transitions and allow for fault recovery
- Mapped a simple file system for paging, persistent storage, and terminal-based program execution

Duck Hunt on FPGA | *SystemVerilog* | *FPGA* | *Intel Quartus Prime* | *USB* | *Device Drivers*

- Implemented Duck Hunt (1984) on an Intel FPGA using SystemVerilog and C
- Synthesized FSM-based hardware modules for game state management and peripheral drivers for mouse and keyboard input and VGA output
- Validated VGA timing constraints and FSM correctness through simulation and on-board FPGA testing

Fingerprint Scanner Garage Door Opener | *C* | *UART* | *ATmega128 Microcontroller*

- Spearheaded the construction of a fingerprint scanner-enabled garage door opener by pitching an IP44-equivalent specification, securing materials funding, and coordinating timely construction
- Ported and optimized fingerprint authentication libraries for the ATmega128 by implementing UART-based communication and interrupt-driven control, thus enabling reliable authentication for 8 stored fingerprints

Experience

Code Ninjas | *Head Instructor* | Arlington Heights, IL — Apr 2023 – Current

- Directed instruction for K–12 students in programming and game development across Scratch, MakeCode, JavaScript, C#, Lua, and Unity by creating a streamlined curriculum based on internal documents
- Directed classroom instruction independently in understaffed conditions, covering workloads typically assigned to 2–3 instructors
- Created new technical documentation to explain core programming concepts and tools for students and parents at home to consume the material in $\leq$50% of the time previously required
- Maintained and upgraded a 40-PC lab environment, reducing external IT labor costs by around $3,000